Claims 3, 4, 6, 9, 10, 12, 22, and 23 are presently active, claims 2, 5, 8, and 11 having been cancelled by this amendment, and new claims 22 and 23 added by this amendment.

In the office action dated 28 August 2002 ("Office Action"), claims 2, 4, 8, and 10 were rejected under 35 U.S.C. §102(b) as being anticipated by Sudo et al., U.S. patent 5,812,018 ("Sudo"); claims 3, 5, 9, and 11 were rejected under 35 U.S.C. §103(a) as being unpatentable over Sudo; and claims 6 and 12 were rejected under 35 U.S.C. §103(a) as being unpatentable over the admitted prior art (Figs. 1-4 in the present application), in view of Nakano, U.S. patent 5,917,366 ("Nakano").

35 U.S.C. §102(b) rejection of claims 2, 4, 8, and 10 over Sudo

The rejections of claims 2 and 8 are now moot because of their cancellation.

Claim 4 is amended to include the limitation of claim 5 that the FET has a leakage current in excess of 1 micro ampere per micron of device width. (Claim 4 is also amended so that the sampling of the output voltage provides a local time-average maximum of the input signal voltage.) By including the limitation of claim 5, it should be clear that claim 4 is not anticipated by Sudo because nowhere does Sudo teach that the FET has a leakage current in excess of 1 micro ampere per micron of device width.

Claim 10 is amended in similar fashion to claim 4, so that for the same reasons as given with respect to claim 4, claim 10 is not anticipated by Sudo.

35 U.S.C. §103(a) rejection of claims 3, 5, 9, and 11 over Sudo

The rejection of claims 5 and 11 are moot because of their cancellation.

Because claim 4 is amended to include the limitation of claim 5, and claim 10 is amended to include the limitation of claim 11, the 35 U.S.C. §103(a) rejection of claims 5 and 11 will also be assumed to be applied to amended claims 4 and 10, respectively.

Claims 3, 4, 9, and 10 recite the limitation that the FET has a leakage current in excess of 1 micro ampere per micron of device width. It is argued in the Office Action, item no. 5 on pages 3 - 4, that it would have been obvious "to set the leakage current for meeting the specific condition which is in each case optimally matched to its application." The Office Action does not state that this setting of the leakage current is

motivated or suggested by Sudo. Sudo is cited only because it is argued that it teaches all the claimed limitations except for the limitation regarding the leakage current and device width.

First, Sudo does not teach all the limitations except for the limitation regarding the leakage current and device width. Claims 3 and 4 recite that the first terminal and gate of the FET are connected to each other and to the input port, and that the second terminal of the FET is connected to the output port. It is argued in the Office Action, page 5, that "connected" should be understood to mean that there may be intermediate elements. Applicant respectfully disagrees with this. It is standard convention in the art of circuit design that the phrase "A is connected to B" means that A and B are connected by an interconnect. It does not mean that they are "connected" to each other via one or more intermediate elements, such as transistors. Usually, the term of art "coupled" is used to indicate the latter case. Note that in Fig. 1 of Sudo, the "second terminal" of transistor M11 is not connected to output port Vpp.

Furthermore, claim 4 recites that the output voltage is sampled at the output port to provide a local time-average maximum of the input signal voltage. But as discussed in the previous office response, Sudo teaches how a negative high voltage VBB and a positive high voltage VPP may be generated from the power supply voltage VCC. (See Sudo, the Abstract and column 1, lines 37 - 67.) Nowhere does Sudo teach a circuit having an output voltage that is indicative of a local time-average maximum. The negative high voltage VBB is not a local time-average maximum of the positive high voltage VPP or the power supply voltage VCC, and the positive high voltage VPP is not a local time-average maximum of the negative high voltage VBB or the power supply voltage VCC.

Claims 9 and 10 both recite the limitation that the gate and the second terminal of the FET are each connected to the output port. Fig. 1 of Sudo clearly does not teach this. The gate of transistor M11 is not connected to the output port. Claim 10 also recites the limitation that the output voltage is sampled at the output port to provide a local time-average minimum of the input signal voltage. Nowhere does Sudo teach this limitation.

Thus, Applicant does not believe that Sudo teaches all of the claimed limitations except for the limitation regarding the leakage current and device width.

Second, Applicant finds the obviousness argument difficult to understand. Why would it be obvious to design an FET to have a leakage current in excess of 1 micro ampere per micron of device width? There is no reference pointed to by the Office Action that makes such a limitation obvious. As Applicant discussed in the previous office response, usually leakage current is something that a circuit designer tries to avoid. This is because for most circuits, leakage current represents wasted power. The present invention is believed novel and nonobvious because it makes use of leakage current to perform maximum or minimum detection of voltage signals.

Accordingly, Applicant believes that claims 3, 4, 9, and 10 are nonobvious in light of Sudo.

35 U.S.C. §103(a) rejection of claims 6 and 12 over the admitted prior art (Figs. 1-4) in view of Nakano

As Applicant discussed in the previous office response, Nakano is cited in the Office Action for teaching field effect transistors that are substituted for diodes. (See the Office Action, top of page 5.) Nowhere does Nakano teach or suggest a FET having a leakage current in excess of 1 micro ampere per micron of device width. As discussed above, this is an important limitation of the invention which Applicant believes is nonobvious.

New claims 22 and 23

New claim 22 is dependent upon claim 3, and adds the limitation that an output circuit is connected to the output port to provide a capacitive load wherein the output voltage is indicative of a local time-average maximum of the input signal voltage. This finds support in Fig. 5 and the specification, paragraph 15, of the present application, where it is indicated that output network 506 is capacitive in nature and loads the output port.

Similar remarks apply to claim 23.

Respeetfully submitted,

Seth Z Kalson Dated: 12-18-02

Seth Z. Kalson
Reg. no. 40,670
Attorney for Applicants and Intel Corporation (Assignee)

Version of Amended Claims Showing Changes

4. (Twice Amended) A method to provide an output voltage indicative of a local time-average maximum of an input signal voltage, the method comprising:

operating a field-effect transistor (FET) in its sub-threshold region when in steady state and the input signal voltage is stationary, the FET having a gate, a first terminal, and a second terminal, wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width, wherein the gate and the first terminal are each connected to an input port, and the second terminal is connected to an output port;

providing the input signal voltage to the input port; and

sampling the output voltage at the output port to provide a local time-average maximum of the input signal voltage.

10. (Twice Amended) A method to provide an output voltage indicative of a local time-average minimum of an input signal voltage, the method comprising:

operating a field-effect transistor (FET) in its sub-threshold region when in steady state and the input signal voltage is stationary, the FET having a gate, a first terminal, and a second terminal, wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width, wherein the first terminal is connected to an input port, and the gate and the second terminal are each connected to an output port;

providing the input signal voltage to the input port; and

sampling the output voltage at the output port to provide a local time-average minimum of the input signal voltage.

Attorney's Docket No.: 42390.P11206 Patent

In re the Application of: Krishnamurthy Soumyanath, et al.
(inventor(s))

Application No.: 09/896,345

Filed: June 28, 2001

For: AREA EFFICIENT WAVEFORM EVALUATION AND DC OFFSET CANCELLATION CIRCUITS
(title)

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

SIR: Transmitted herewith is an Amendment for the above application.

_____ Small entity status of this application under 37 C.F.R. §§ 1.9 and 1.27 has been established by a verified statement previously submitted.
_____ A verified statement to establish small entity status under 37 C.F.R. §§ 1.9 and 1.27 is enclosed.
_____ No additional fee is required.
X RCE Transmittal and fee required under 37 C.F.R. § 1.17(e)

The fee has been calculated as shown below:

	(Col. 1) Claims Remaining After Amd.		(Col. 2) Highest No. Previously Paid For	(Col. 3) Present Extra
Total Claims	* 8	Minus	** 21	0
Indep. Claims	* 6	Minus	*** 8	0
☐	First Presentation of Multiple Dependent Claim(s)			

	SMALL ENTITY Rate	Additional Fee	OTHER THAN A SMALL ENTITY Rate	Additional Fee
	X9	$	X18	$ 0
	X42	$	X84	$ 0
	+140	$	+280	$
	Total Add. Fee	$	Total Add. Fee	$ 0

* If the entry in Col. 1 is less than the entry In Col. 2, write "0" in Col. 3.

** If the "Highest No. Previously Paid For" IN THIS SPACE is less than 20, write "20" in this space.

*** If the "Highest No. Previously Paid For" IN THIS SPACE is less than 3, write "3" in this space. The "Highest No. Previously Paid For" (Total or Independent) is the highest number found from the equivalent box in Col. 1 of a prior amendment or the number of claims originally filed.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231

on December 18, 2002.
Date of Deposit

Carrie Boccaccini
Name of Person Mailing Correspondence

Carrie Boccaccini 12-18-2002
Signature Date

(TNF/pab 10/01/01)

____ A check in the amount of $_____ is attached for presentation of additional claim(s).

__X__ Applicant(s) hereby Petition(s) for an Extension of Time of ONE month(s) pursuant to 37 C.F.R. § 1.136(a).

__X__ A check for $ 110.00 is attached for processing fees under 37 C.F.R. § 1.17(i).

____ Please charge my Deposit Account No. 02-2666 the amount of $_____.

A duplicate copy of this sheet is enclosed.

__X__ The Commissioner of Patents and Trademarks is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 02-2666 **(a duplicate copy of this sheet is enclosed)**:

__X__ Any additional filing fees required under 37 C.F.R. § 1.16 for presentation of extra claims.

__X__ Any extension or petition fees under 37 C.F.R. § 1.17.

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

Date: 12-18-02

Seth Z. Kalson

Seth Z. Kalson

Reg. No. 40,670

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(408) 720-8300

(TNF/pab 10/01/01)